FIG. 1

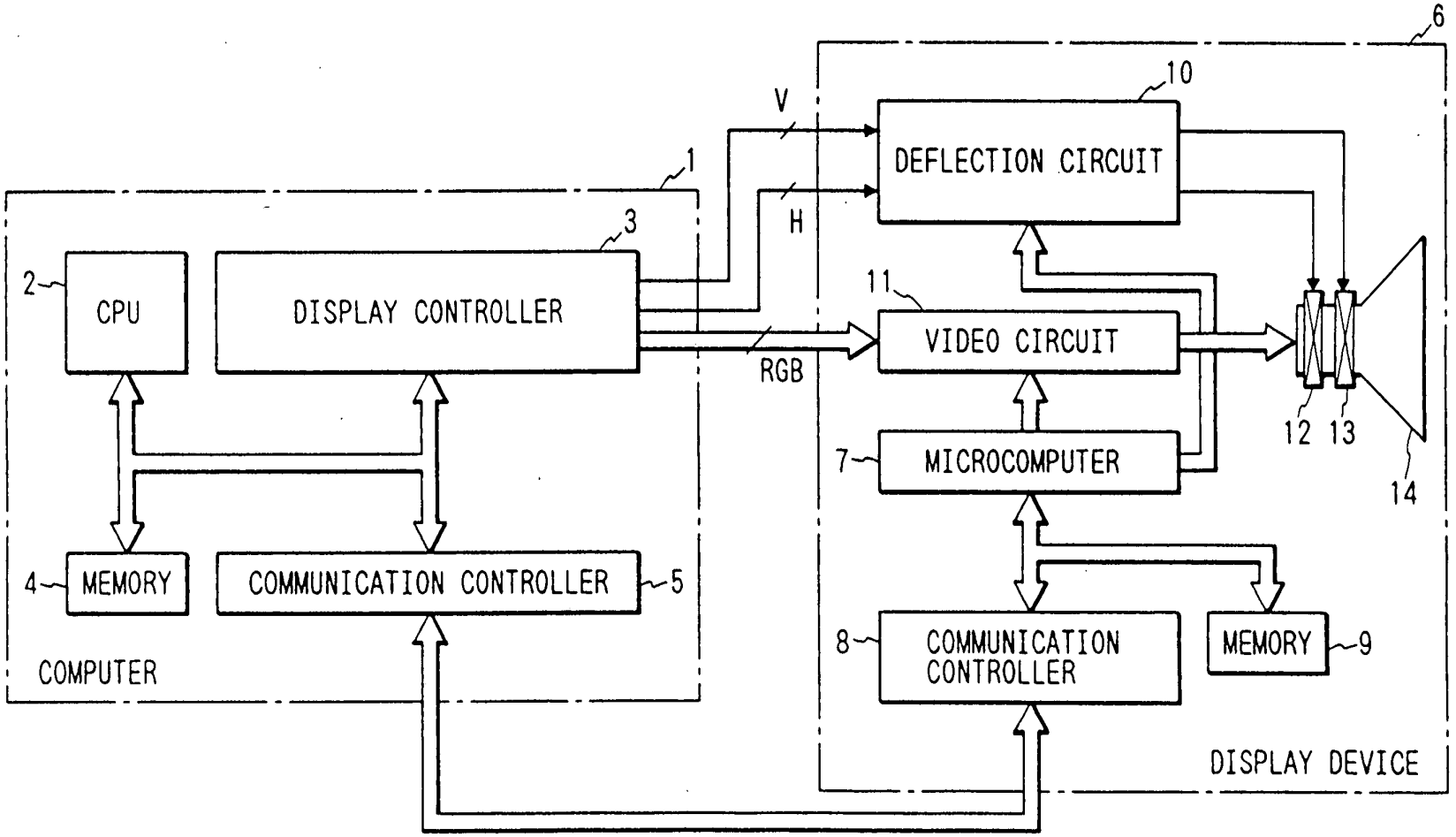

6
10
V
DEFLECTION CIRCUIT
1
H
3
2
CPU
DISPLAY CONTROLLER
11
VIDEO CIRCUIT
RGB
12
13
14
7
MICROCOMPUTER
4
MEMORY
COMMUNICATION CONTROLLER
5
8
COMMUNICATION CONTROLLER
MEMORY
9
COMPUTER
DISPLAY DEVICE

FIG. 2

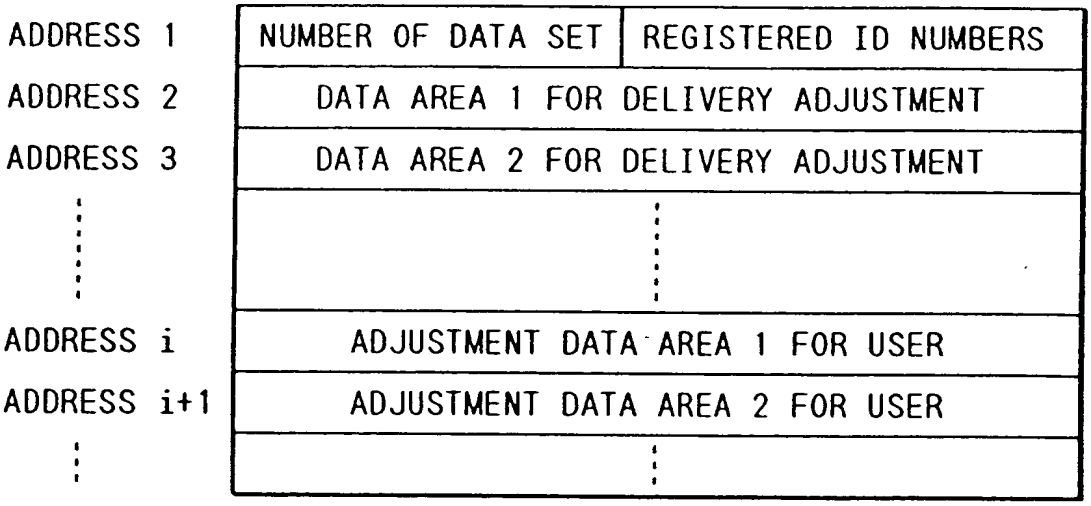

ADDRESS 1
NUMBER OF DATA SET
REGISTERED ID NUMBERS
ADDRESS 2
DATA AREA 1 FOR DELIVERY ADJUSTMENT
ADDRESS 3
DATA AREA 2 FOR DELIVERY ADJUSTMENT
ADDRESS i
ADJUSTMENT DATA AREA 1 FOR USER
ADDRESS i+1
ADJUSTMENT DATA AREA 2 FOR USER

FIG. 3

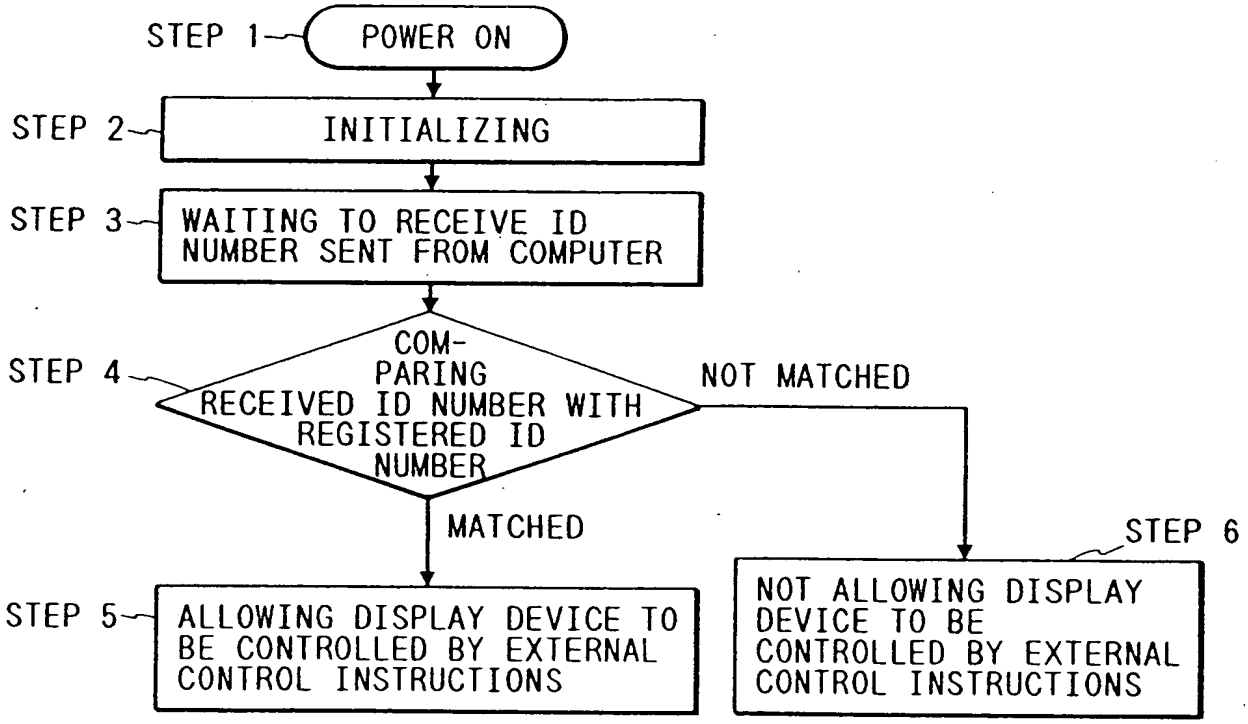

STEP 1
POWER ON
STEP 2
INITIALIZING
STEP 3
WAITING TO RECEIVE ID NUMBER SENT FROM COMPUTER
STEP 4
COM-PARING RECEIVED ID NUMBER WITH REGISTERED ID NUMBER
NOT MATCHED
MATCHED
STEP 5
ALLOWING DISPLAY DEVICE TO BE CONTROLLED BY EXTERNAL CONTROL INSTRUCTIONS
STEP 6
NOT ALLOWING DISPLAY DEVICE TO BE CONTROLLED BY EXTERNAL CONTROL INSTRUCTIONS

FIG. 4

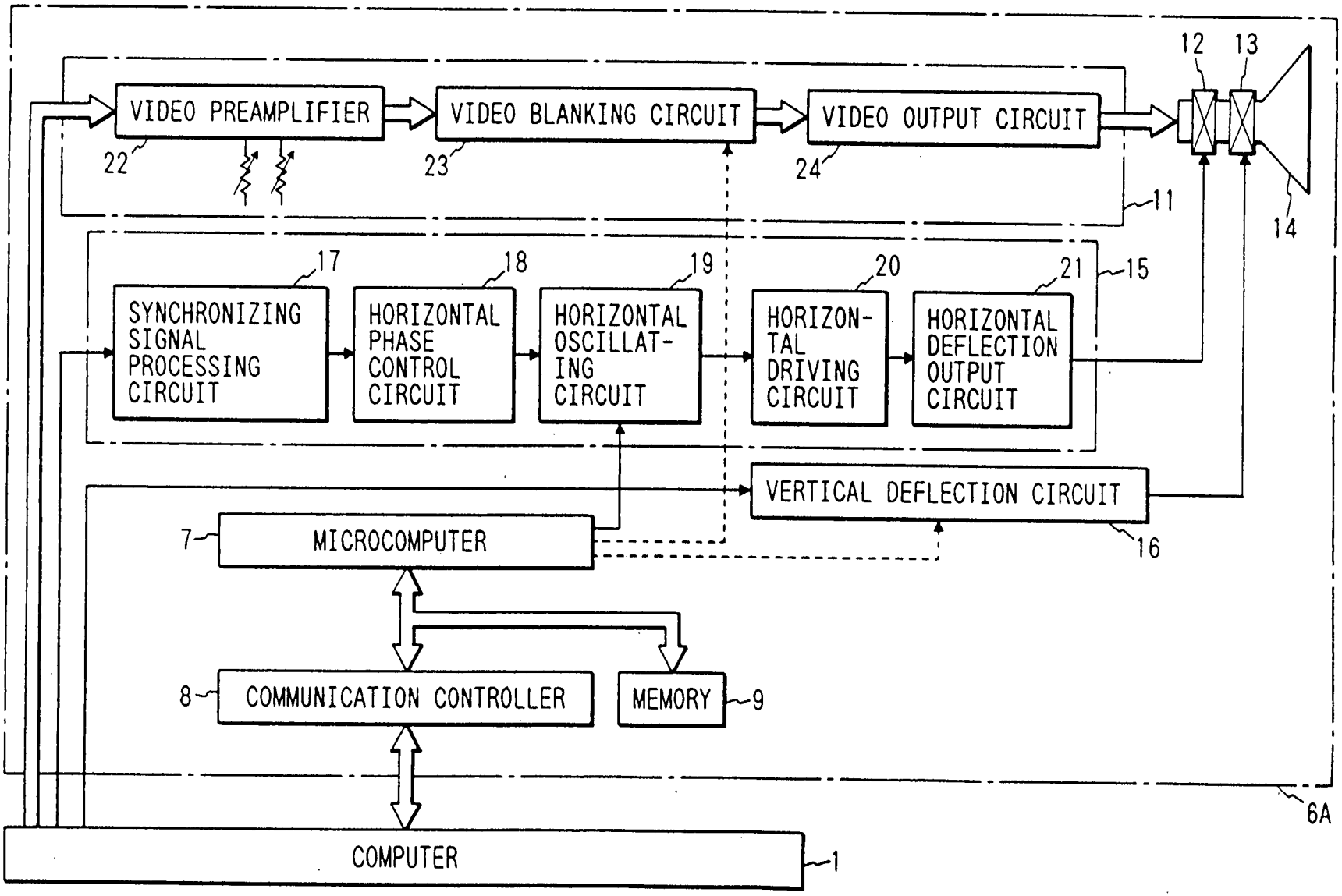

VIDEO PREAMPLIFIER
VIDEO BLANKING CIRCUIT
VIDEO OUTPUT CIRCUIT
12
13
14
22
23
24
11
15
17
18
19
20
21
SYNCHRONIZING SIGNAL PROCESSING CIRCUIT
HORIZONTAL PHASE CONTROL CIRCUIT
HORIZONTAL OSCILLATING CIRCUIT
HORIZONTAL DRIVING CIRCUIT
HORIZONTAL DEFLECTION OUTPUT CIRCUIT
VERTICAL DEFLECTION CIRCUIT
16
7
MICROCOMPUTER
8
COMMUNICATION CONTROLLER
MEMORY
9
6A
COMPUTER
1

FIG. 5

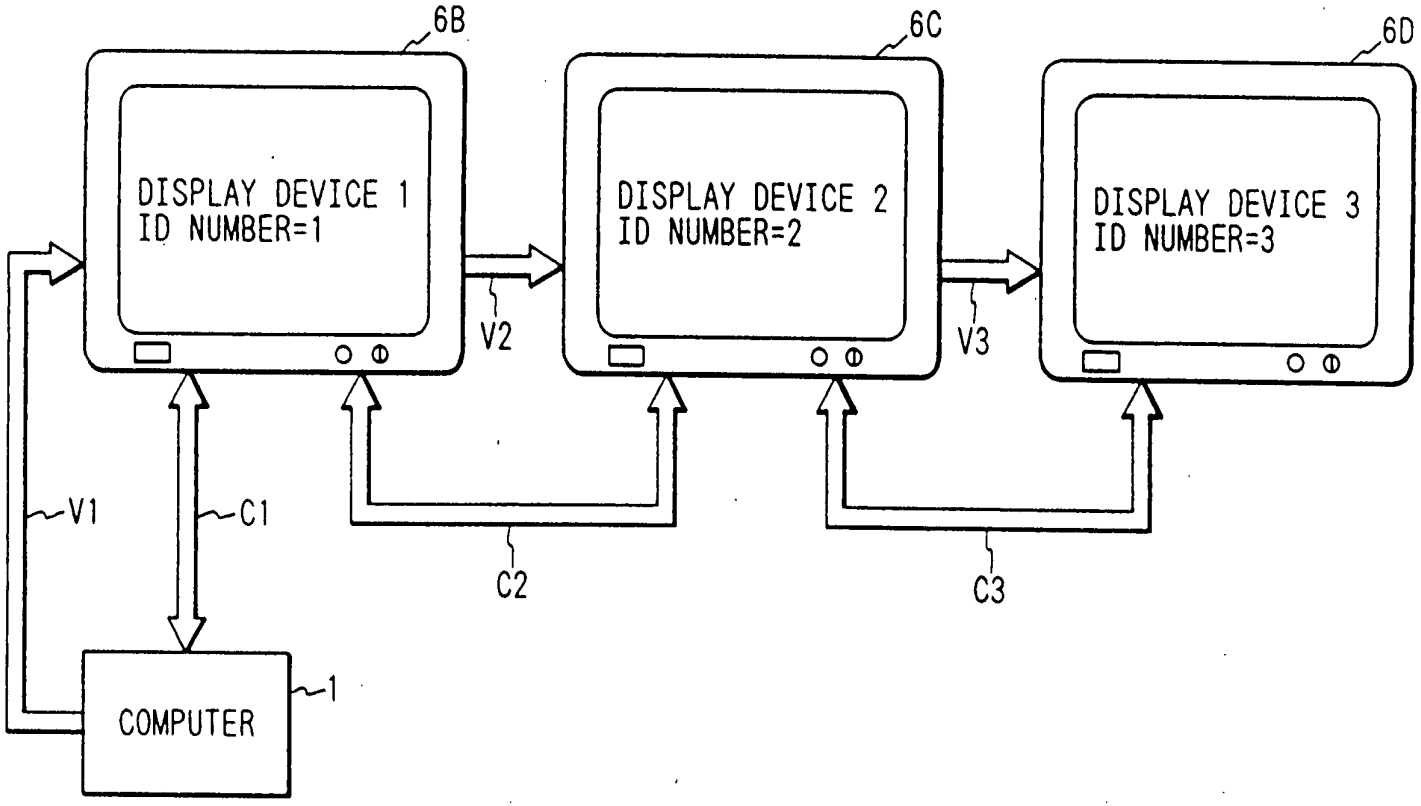

6B
6C
6D
DISPLAY DEVICE 1
ID NUMBER=1
DISPLAY DEVICE 2
ID NUMBER=2
DISPLAY DEVICE 3
ID NUMBER=3
V1
V2
V3
C1
C2
C3
COMPUTER
1

FIG. 6

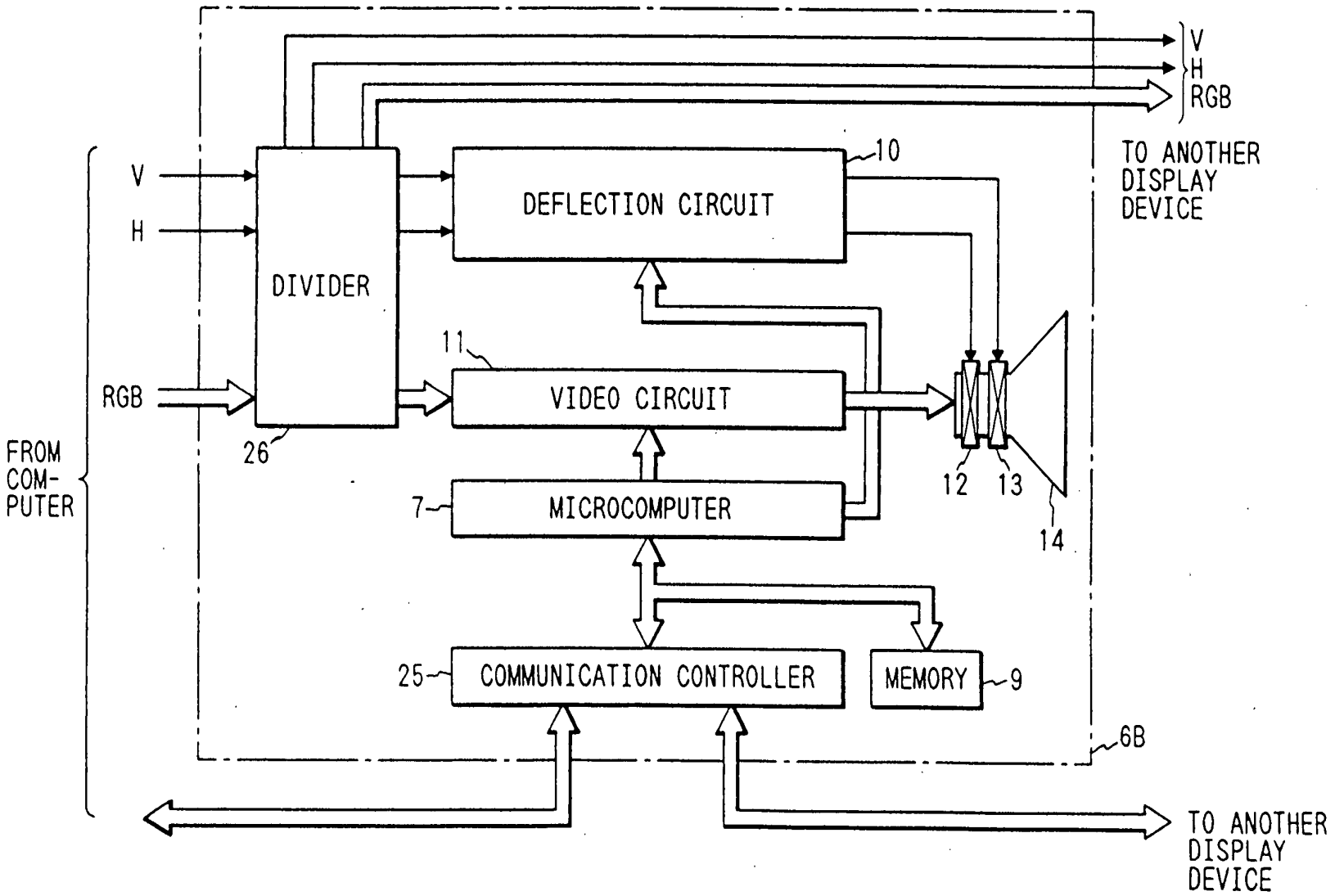

V
H
RGB
TO ANOTHER DISPLAY DEVICE
V
H
DIVIDER
10
DEFLECTION CIRCUIT
RGB
11
VIDEO CIRCUIT
26
FROM COM-PUTER
7
MICROCOMPUTER
12
13
14
25
COMMUNICATION CONTROLLER
MEMORY
9
6B
TO ANOTHER DISPLAY DEVICE

FIG. 7

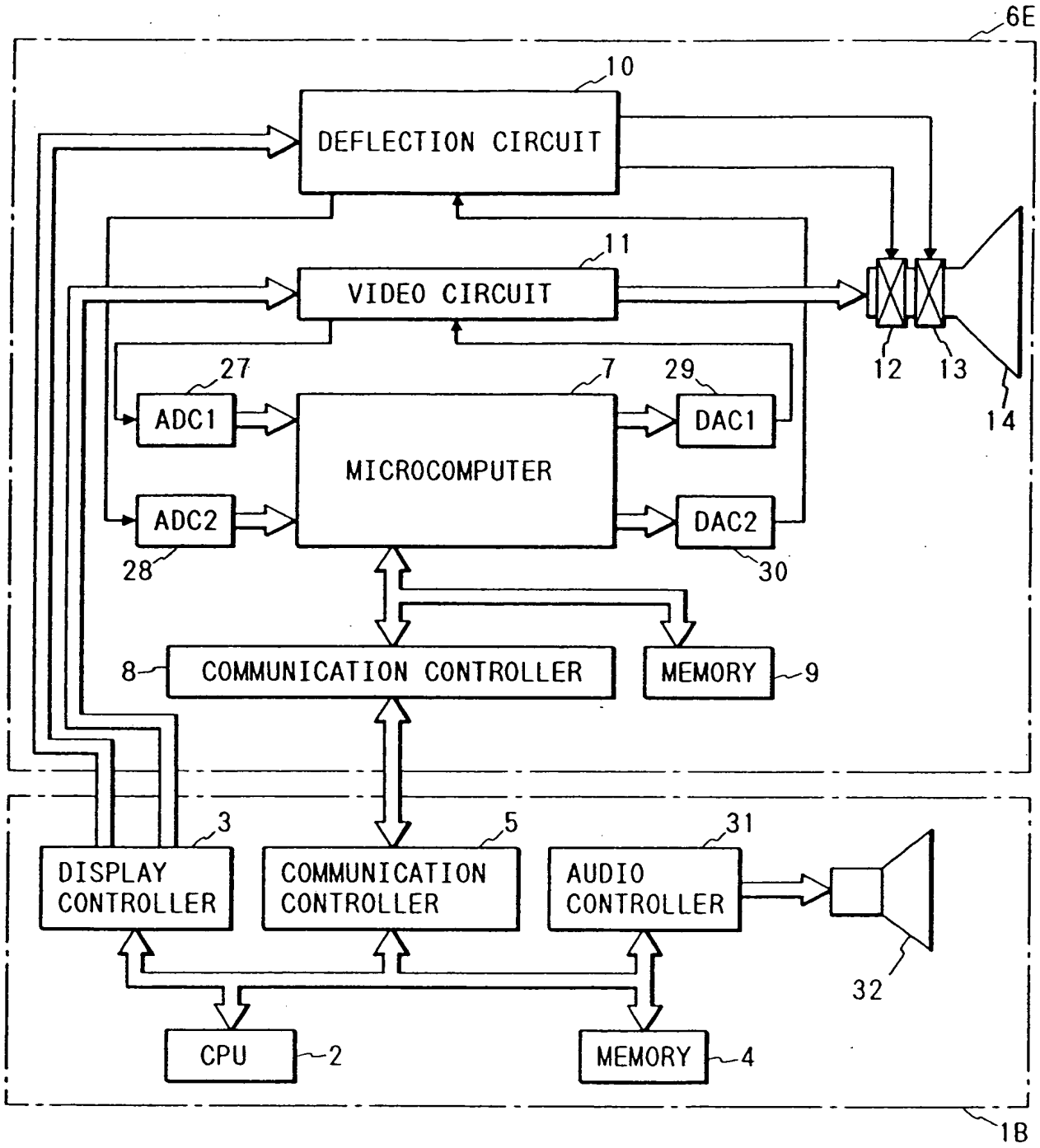

6E
10
DEFLECTION CIRCUIT
11
VIDEO CIRCUIT
12
13
14
27
ADC1
7
MICROCOMPUTER
29
DAC1
ADC2
DAC2
28
30
8
COMMUNICATION CONTROLLER
MEMORY
9
3
DISPLAY CONTROLLER
5
COMMUNICATION CONTROLLER
31
AUDIO CONTROLLER
32
CPU
2
MEMORY
4
1B

FIG. 8

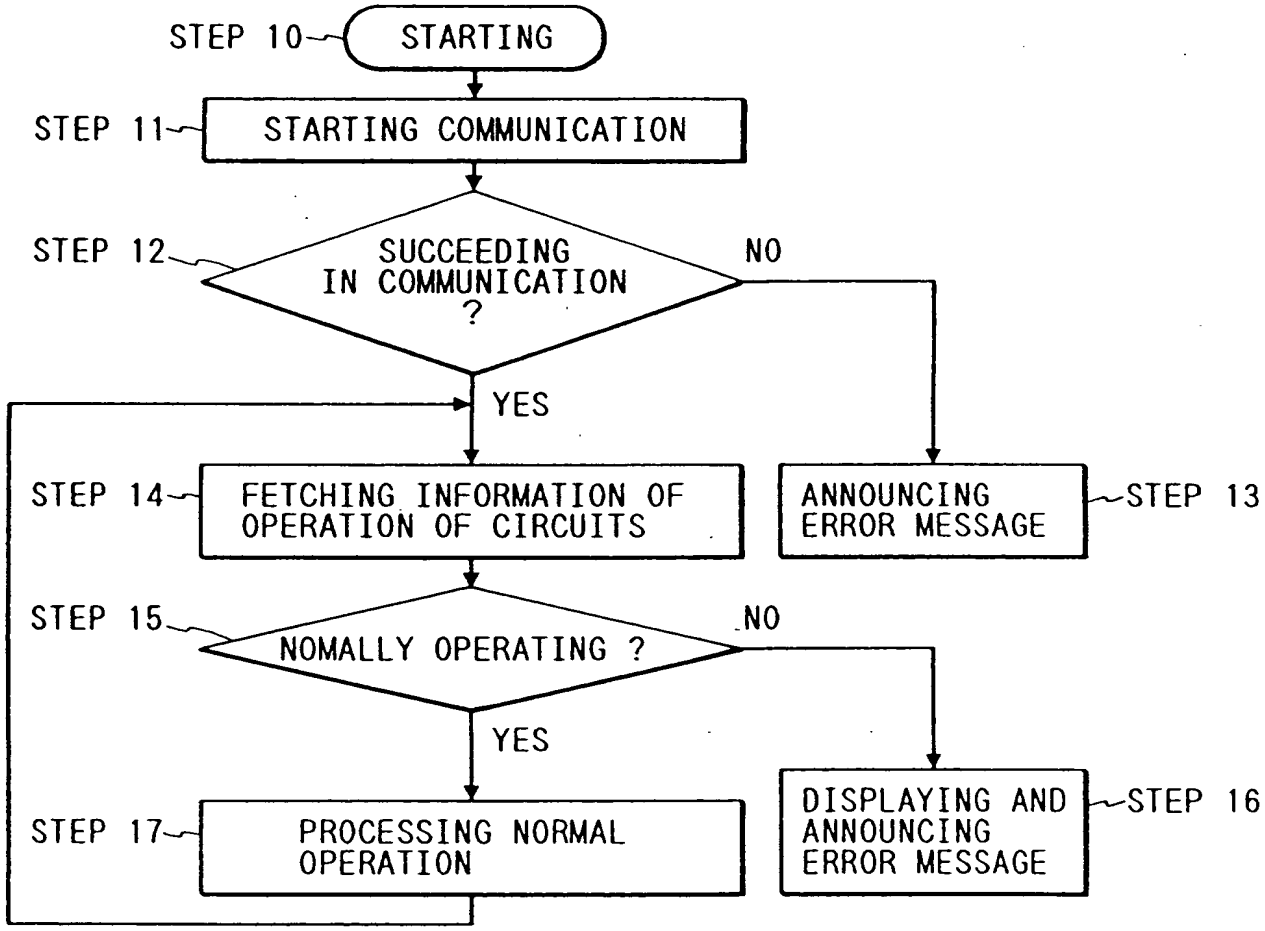

STEP 10
STARTING
STEP 11
STARTING COMMUNICATION
STEP 12
SUCCEEDING IN COMMUNICATION ?
NO
YES
STEP 14
FETCHING INFORMATION OF OPERATION OF CIRCUITS
ANNOUNCING ERROR MESSAGE
STEP 13
STEP 15
NOMALLY OPERATING ?
NO
YES
STEP 17
PROCESSING NORMAL OPERATION
DISPLAYING AND ANNOUNCING ERROR MESSAGE
STEP 16

FIG. 9

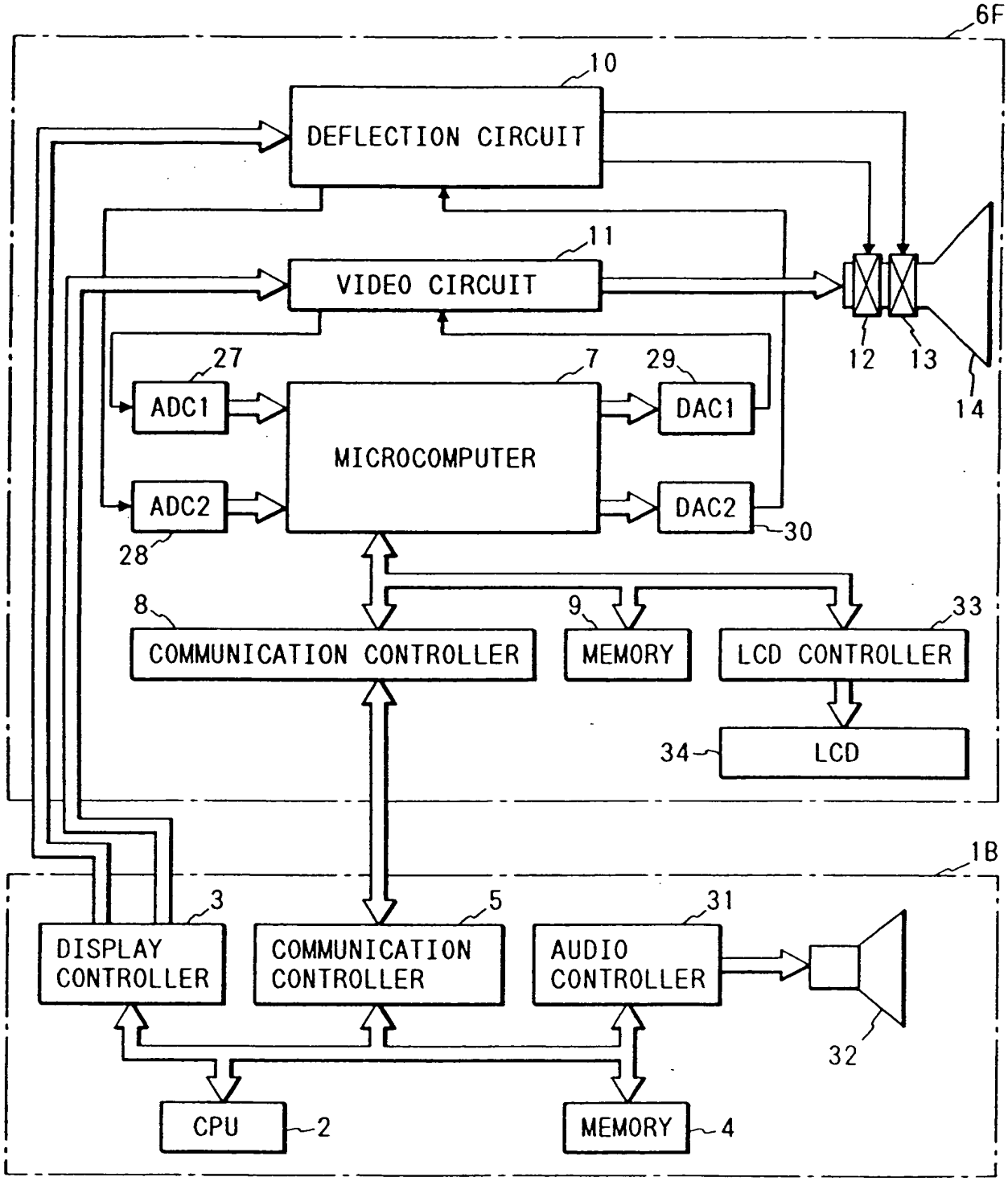

6F
10
DEFLECTION CIRCUIT
11
VIDEO CIRCUIT
12
13
14
27
ADC1
7
MICROCOMPUTER
29
DAC1
ADC2
DAC2
30
28
8
COMMUNICATION CONTROLLER
9
MEMORY
33
LCD CONTROLLER
34
LCD
1B
3
DISPLAY CONTROLLER
5
COMMUNICATION CONTROLLER
31
AUDIO CONTROLLER
32
CPU
2
MEMORY
4

FIG. 10

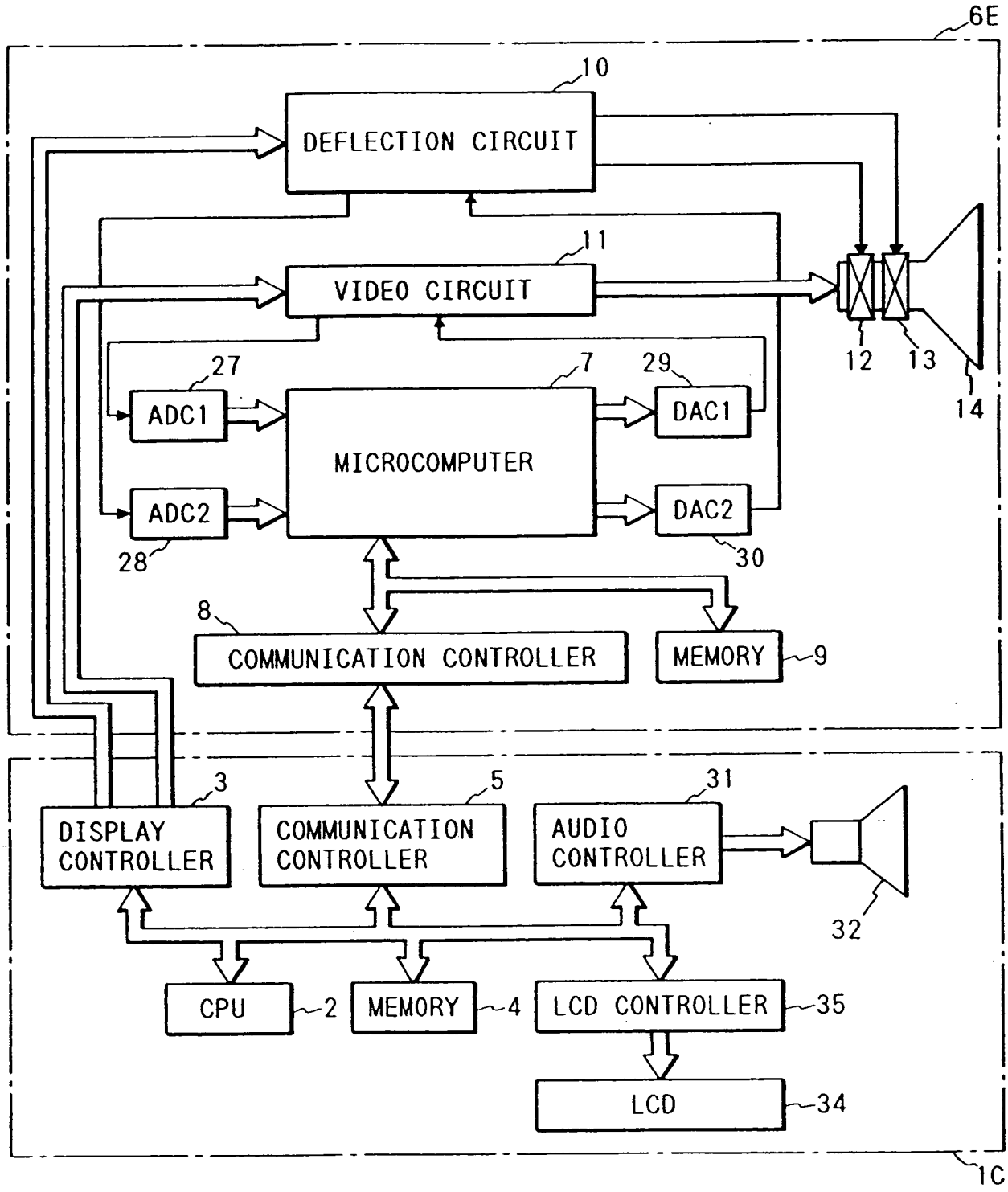

6E
10
DEFLECTION CIRCUIT
11
VIDEO CIRCUIT
12
13
14
27
ADC1
7
MICROCOMPUTER
29
DAC1
ADC2
DAC2
28
30
8
COMMUNICATION CONTROLLER
MEMORY
9
3
DISPLAY CONTROLLER
5
COMMUNICATION CONTROLLER
31
AUDIO CONTROLLER
32
CPU
2
MEMORY
4
LCD CONTROLLER
35
LCD
34
1C

FIG. 11

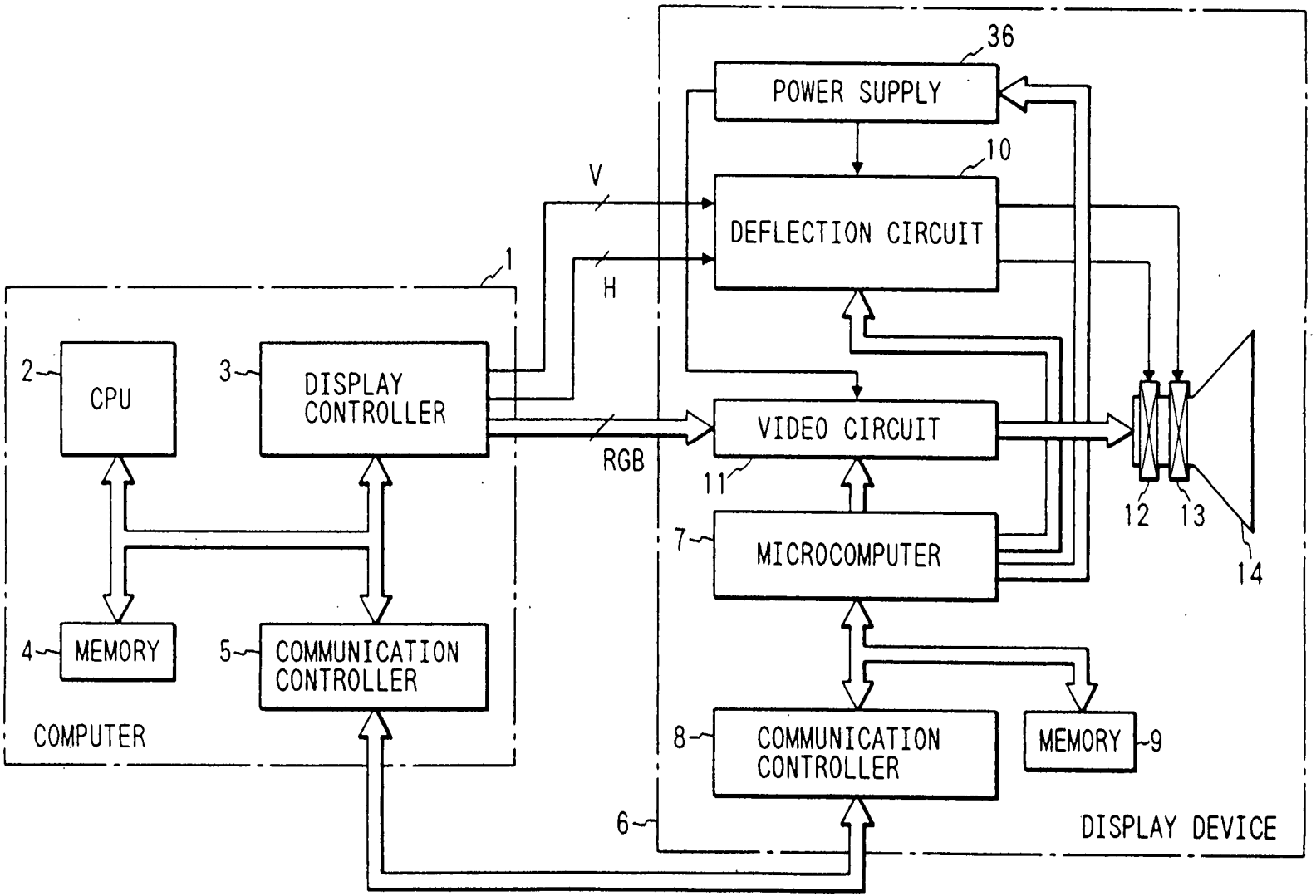
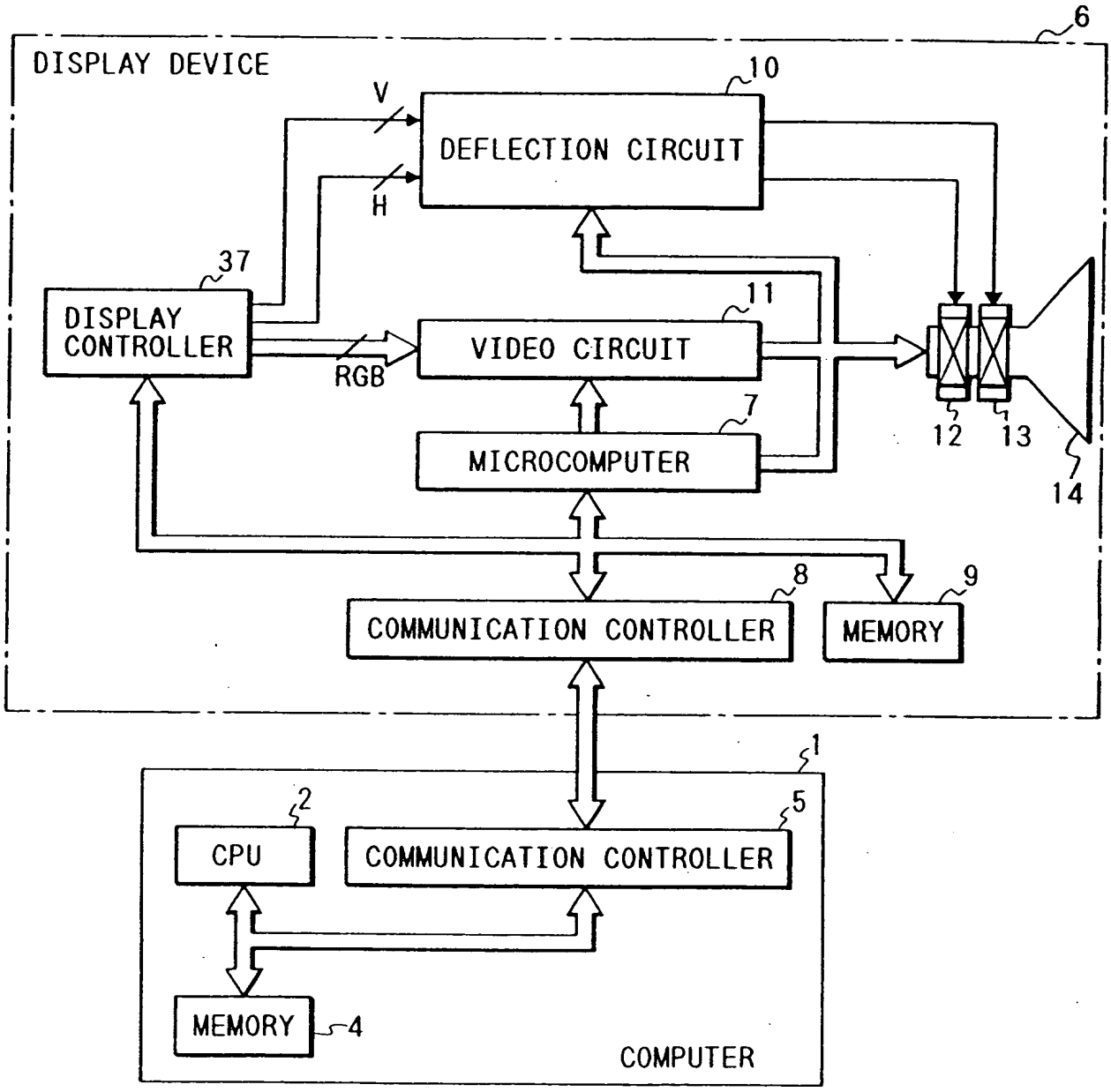

36
POWER SUPPLY
10
DEFLECTION CIRCUIT
V
H
1
2
CPU
3
DISPLAY CONTROLLER
RGB
VIDEO CIRCUIT
11
12
13
14
7
MICROCOMPUTER
4
MEMORY
5
COMMUNICATION CONTROLLER
COMPUTER
8
COMMUNICATION CONTROLLER
MEMORY
9
6
DISPLAY DEVICE

FIG. 12


6
DISPLAY DEVICE
10
V
DEFLECTION CIRCUIT
H
37
DISPLAY CONTROLLER
11
VIDEO CIRCUIT
RGB
7
MICROCOMPUTER
12
13
14
8
COMMUNICATION CONTROLLER
9
MEMORY
1
2
CPU
5
COMMUNICATION CONTROLLER
MEMORY
4
COMPUTER